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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,227	10/22/2001	Gerald Deboy	GR 99 P 1679	8514

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EXAMINER
ROSE, KIESHA L

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,227	DEBOY ET AL.	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed 7 June 2004.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4,7-9,11-15 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barret et al. (U.S. Patent 5,780,895) in view of Nandakumar et al. (U.S. Patent 5,296,725).

Barret discloses a vertical semiconductor component (Fig. 3) that contains a substrate (0) of a first conductivity (N) having a first and second side, an insulating layer (8) covering first side and having a side remote from substrate, a more highly doped layer (11) of first conductivity applied on second side, a metallic drain contact (12) applied on the more highly doped layer, a metallic gate contact, a multiplicity of MOS cells on first side of substrate for forming a first semiconductor switch, each MOS cell having a first well (1) of the second conductivity (P) and being introduced into the substrate and reaching first side and extending orthogonally from the first side to the second side, a first metallic source contact (3) extended through insulating layer, a first source (2) of first conductivity being incorporated into well and having a potential,

reaching to first side of substrate and connecting to first source metallic contact, a first gate (6) on side of insulating layer remote to the substrate and partly covering well and connecting to metallic gate contact, a plurality of further MOS cells identical to multiplicity of MOS cells having a second well, source, gate and source contact and connected in a cascaded manner. Barret discloses all the limitations except for a region incorporated in the substrate of second conductivity type. Whereas Nandakumar discloses a switching device (Figs. 3 and 6b) that contain a substrate with a drain region (14) with a drain contact (13), a well (34) with a source region (40) a gate (38) and a region (33) of second conductivity type laterally insulated and formed orthogonally and incorporated into the substrate by a cascaded manner and holds charge and reaching to the first side and electrically connected to the gate in the MOS cell and having a potential floating relative to the potential of the source where a space charge zone is defined between the MOS cells and region , the region is surrounded by the MOS cells to form a switching device and a MOS cell is surrounded by the region (Fig. 6b). The region is formed to act as diverted and provides the mean of the turn-on and turn-off controls. (Column 8, lines 8-10) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor component by incorporating a region as a diverter and to control turn-on and turn-off of the device as taught by Nandakumar.

Claims 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barret, Nandakumar as applied to claims 1,2 and 7 above, and further in view of Liao et al. (U.S. Patent 6,359,309).

Barret and Nandakumar disclose all the limitations except for a lateral insulation between MOS cells. Whereas Liao discloses a power device (Fig. 3) that contains MOS cells with a lateral insulation (4) formed therebetween. The lateral insulation is formed so when power is applied to gate a channel is formed and the device is turned on. (Column 1, lines 43-45) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Barret and Nandakumar by incorporating a lateral insulation to provide a voltage to turn the device on as taught by Liao.

Response to Arguments

Applicant's arguments filed 7 June 2004 have been fully considered but they are not persuasive. Applicant argues that the Barret and Nandakumar references do not disclose a second conductivity type region in the semiconductor substrate that contacts the gate electrode, this is erroneous the Nandakumar reference discloses a substrate with a second conductivity type region (33) formed therein and a first gate (46) and a second gate (38) where the second conductivity type region does contact the gate electrode. (Fig. 3) Therefore the rejection stands. In addition the applicant argues that the reference can not be combined since the Barret reference is a transistor and the Nandakumar reference is a thyristor. A thyristor is a form of a transistor and in addition of transistor of Barret is a power transistor and a thyristor is a power transistor. Therefore the references can be combined.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

KLR

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800